Full Chip CDM Simulation With Package Layout Included for Connectivity and Charge Distribution

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Biography

- Career
  - Started EE Career at ON Semiconductor in March 2008 as design intern
  - ON Semiconductor ESD discrete device & process designer, 2009 - 2017
  - Samsung Electronics, HQ, Foundry Division, ESD verification focusing on deployment of full chip CDM for FA and signoff 2017 - present
- Education
  - B.S.E in electrical engineering in 2009, Arizona State University
  - M.S.E in electrical engineering in 2015, Arizona State University
- Pastime
  - Camping, exploring Korea, church, and my 6.9 children

Abstract

There are several advanced EDA tools that can simulate full chip CDM stress. However, they only take into account the IC layout through the use of GDS, CCI, or SVDB databases[1] in order to determine the charge distribution for a related CDM stress level. CDM stress is strongly influenced by package characteristics.[2][3] While inclusion of spice netlist models of the package can improve accuracy in most cases, it cannot account for changes to charge storage distribution when it occurs dominantly on the package metal itself. A process for including the package layout within these simulations is discussed in two cases where chip on film (COF) mounting with film level routing (FLR) is used as the package. The motivation to develop a simulation flow where the package layout can be taken into consideration is to increase the accuracy of charge distribution of the nodes being simulated. By including the package metal as essentially a new top metal layer in the IC layout DB, this and the impact of high resistance FLR traces can be taken into account. The two cases discussed highlight the need of physical package layout inclusion over netlist models while acknowledging that this level of accuracy is only needed in certain package specific cases.

Overview

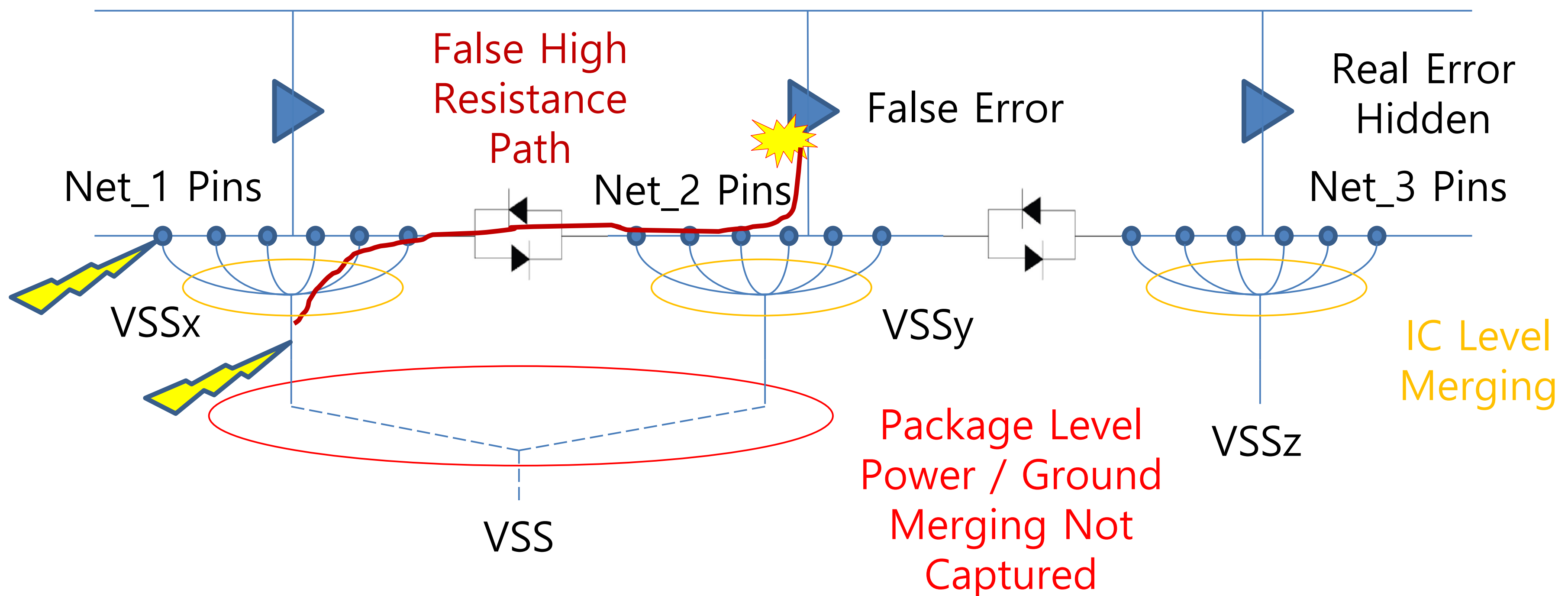
- The Whys:
  - Why is package data needed for full chip CDM?
  - What package data is needed?
  - What makes thin film packaging different?
- The Hows:
  - Overcoming the caveats of full chip CDM for thin film applications
  - The process
- The Cases:
  - Case 1: Physical failure not found without package data
  - Case 2: Physical failure found without package data

Overview

- Full chip CDM simulations can be influenced by the package
- Package attributes that increase influence:
  - Long wires in thin film package increase discharge path resistances
  - Thin film packaging has a dominant effect on CDM charge distribution since packaging is major charge source
- Package Specificities
  - Packages that rely on film layer routing (FLR) can have inherent issues when simulating chip level CDM
  - Resistive models of FLR are not always enough for capturing failures

Package Data Needs In CDM Simulations

- The need for package data in full chip CDM simulations
  - Package level connectivity can strongly influence the CDM current path
  - When no package data available only simple assumptions can be made about connectivity

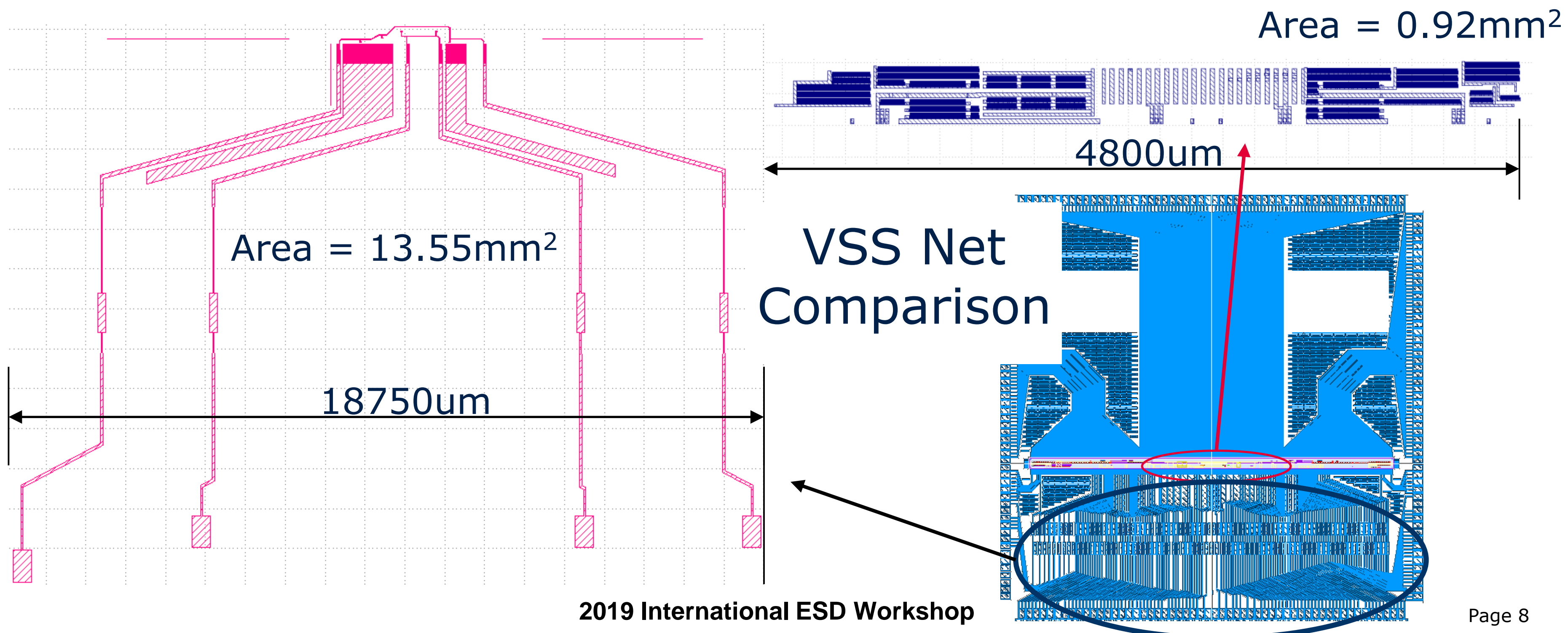


Package Data Needs In CDM Simulations

- The need for package data in thin film cases
  - Package trace resistance can be an issue
    - Ideal connectivity between IC pins and chip pads can provide good results in classical packages where trace resistances are small in comparison to global ESD path resistance.
    - In thin film packaging, trace resistance can be the main ESD path contributor. Thus, package level shorting show far less influence.
  - Charge distribution can be an issue
    - Since package covers significantly larger surface than chip, CDM charge storage distribution will differ significantly between the two, both quantitatively and qualitatively.

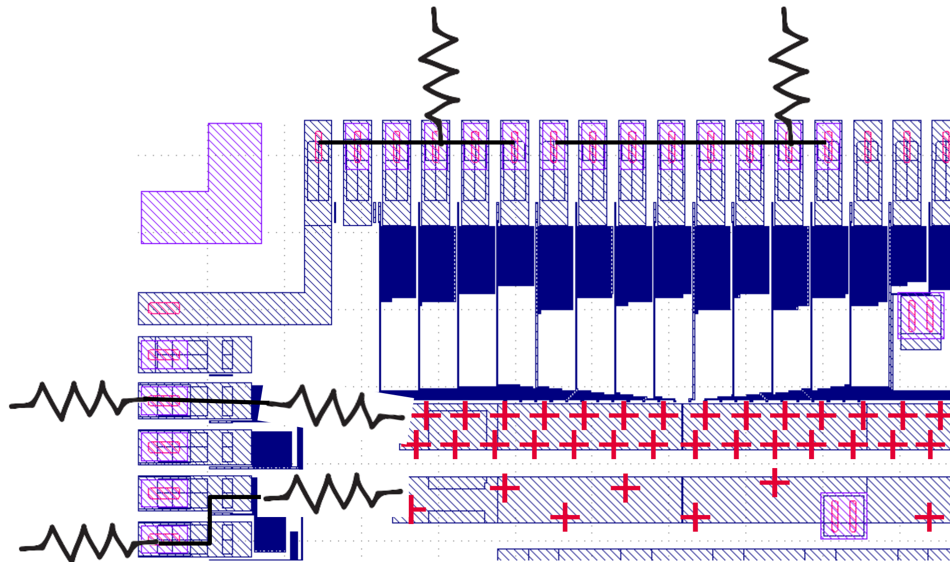
Package Data Needs – Thin Film

- The problem with chip simulations alone
  - FLR packaging orients the IC ‘substrate up’ during CDM testing
  - This orientation applies the charge to the top metal layer
  - When packaging is taken into account, charge distribution is significantly modified due to change in charged surfaces



Package Data Needs – Thin Film

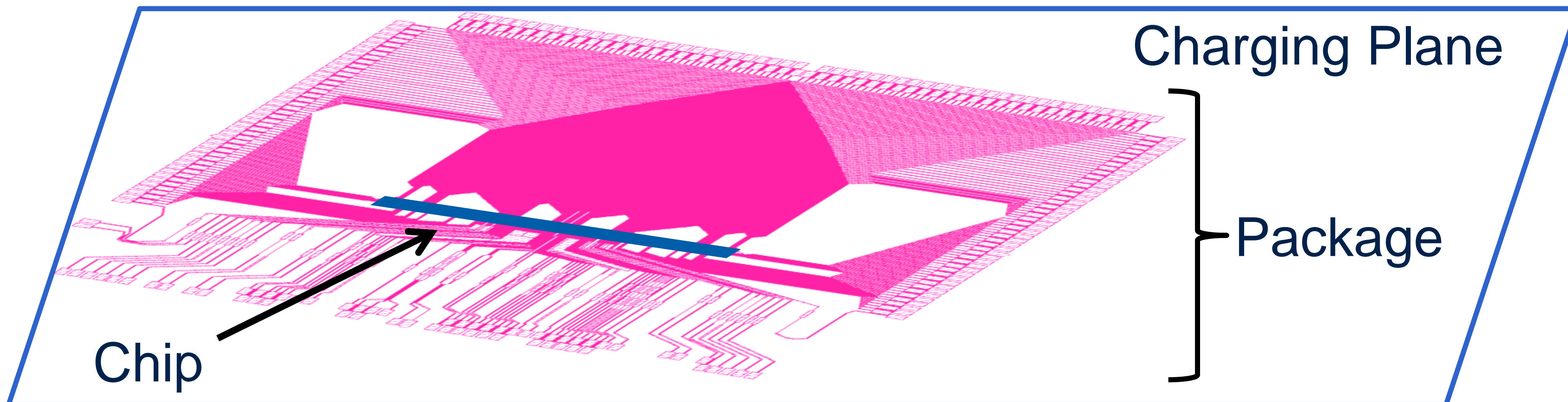
- Package models improve connectivity and ESD path considerations, but don't aide in charge distribution accuracy
  - Resistive package model adds trace resistance to discharge paths
  - Package netlist model does not supply geometric information.
    - Accurate charge distribution estimation can be difficult.
  - No improvement in accuracy of simulation



Connectivity and discharge path resistances are more accurate, but no improvement to overall simulation accuracy

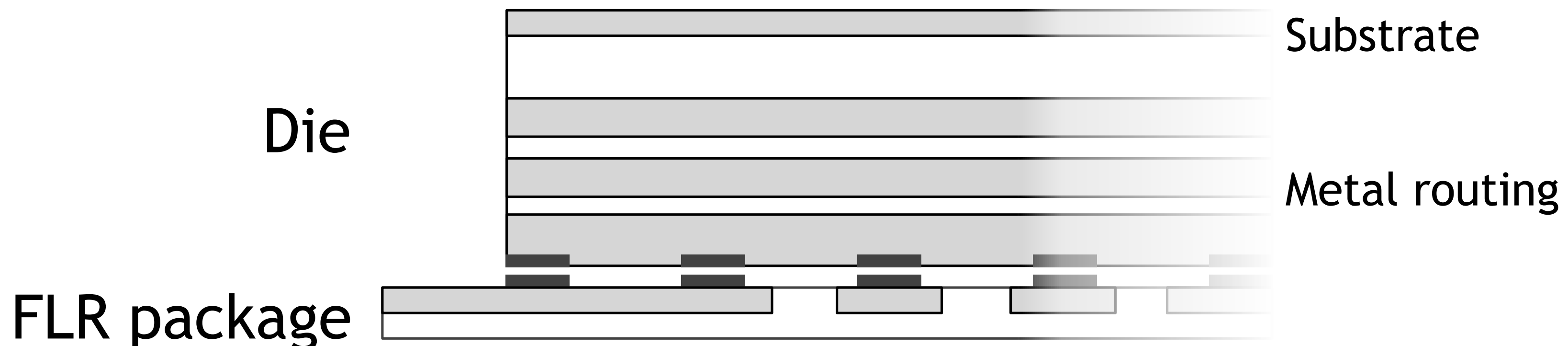
Simulation Methodology – Thin Film

- The Solution: Incorporate layout geometry in simulation DB
  - Resistance model is not needed.
    - Package traces are seen as another layer of interconnect
    - Esra simulation tool automatically calculates resistances for interconnect.
  - Charge distribution is handled accurately for all metal



Simulation Methodology – Thin Film

- Charge distribution is calculated using Silicon Frontline's proprietary model
- Charge distribution for FLR package is based on:
  - Package and IC layer shapes
  - Proximity of shapes to the charged plate
- Accuracy verified through comparison with FA results and silicon

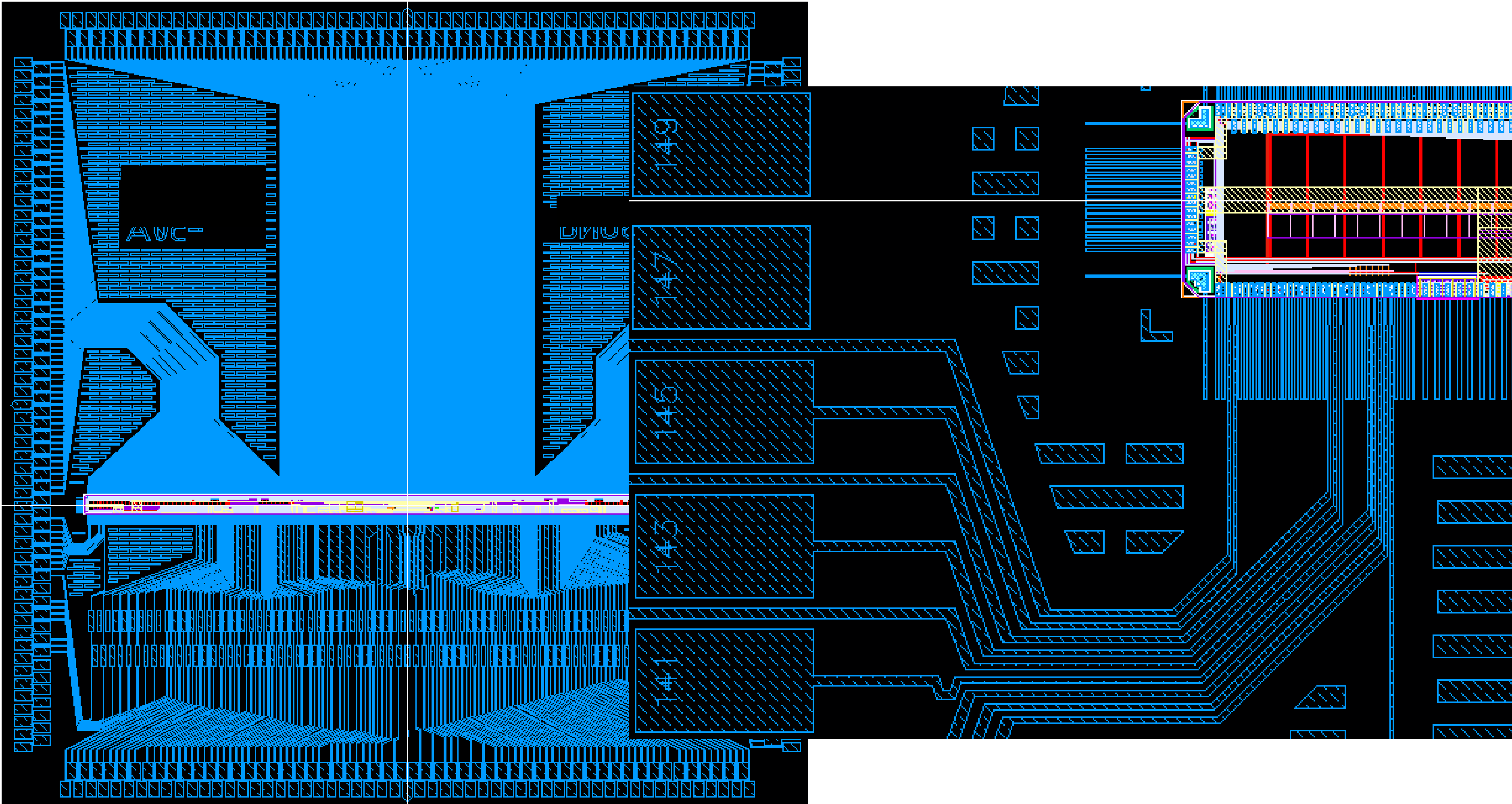


Overcoming the caveats of full chip CDM

- The Solution: It's not trivial…
  - Package layout has to be converted to compatible format
    - AutoCAD dwg → to dxf → to gdsii
  - Scaling and orientation manipulation
    - Typically layout files have 1D scaling coefficient to account for expansion of thin film during mounting
    - Origin and orientation of package and die must align
  - Labor intensive process of converting layout gds to cci DB
  - Combination of LVS generated cci DB of die and package cci DB
  - Modification of technology and mapping files to accommodate "additional" metal layers

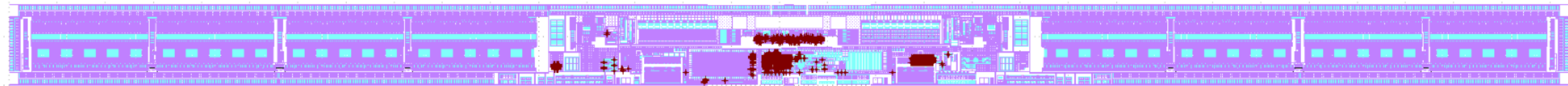
Overcoming the caveats of full chip CDM

- The Result: Fully integrated IC and package layouts
  - Chip on film (COF) with film level routing (FLR) package

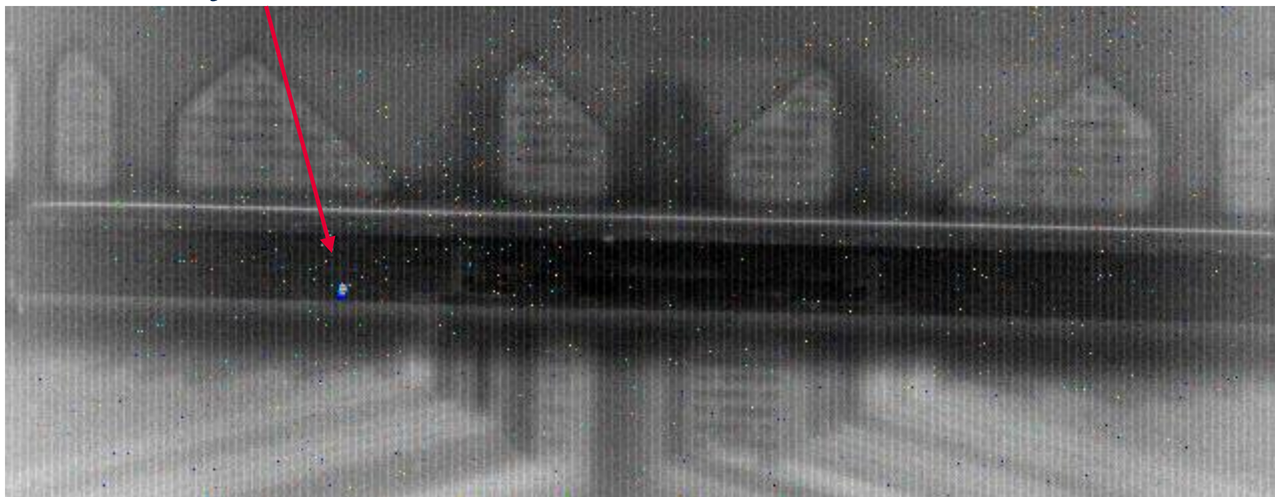


Case 1 – Failure Not Found without Package

- In testing it was found that a display driver IC had CDM failures in a given cell
- Initial simulation findings did not match physical failures
  - Most failures in simulation found near center of die



Fail Locations
Physical / Simulation

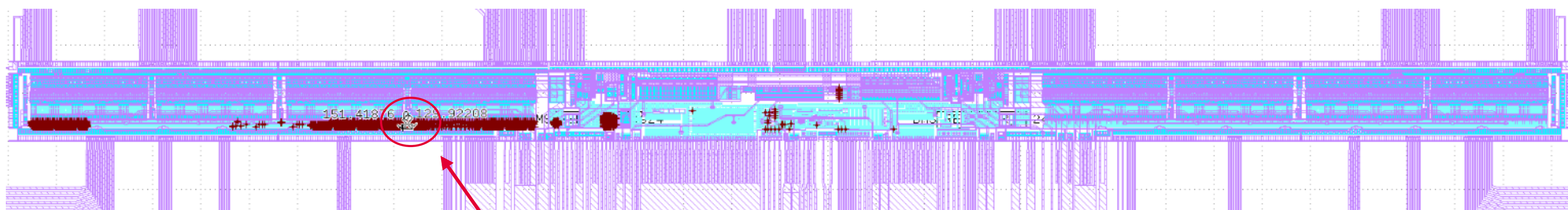


Case 1 – Failure Not Found without Package

- To improve simulation accuracy netlist package model was generated and included
- It was assumed increased discharge path resistance due to package traces was the issue
- Simulated failure locations were still at center of die not matching failure analysis

Case 1 – Failure Not Found without Package

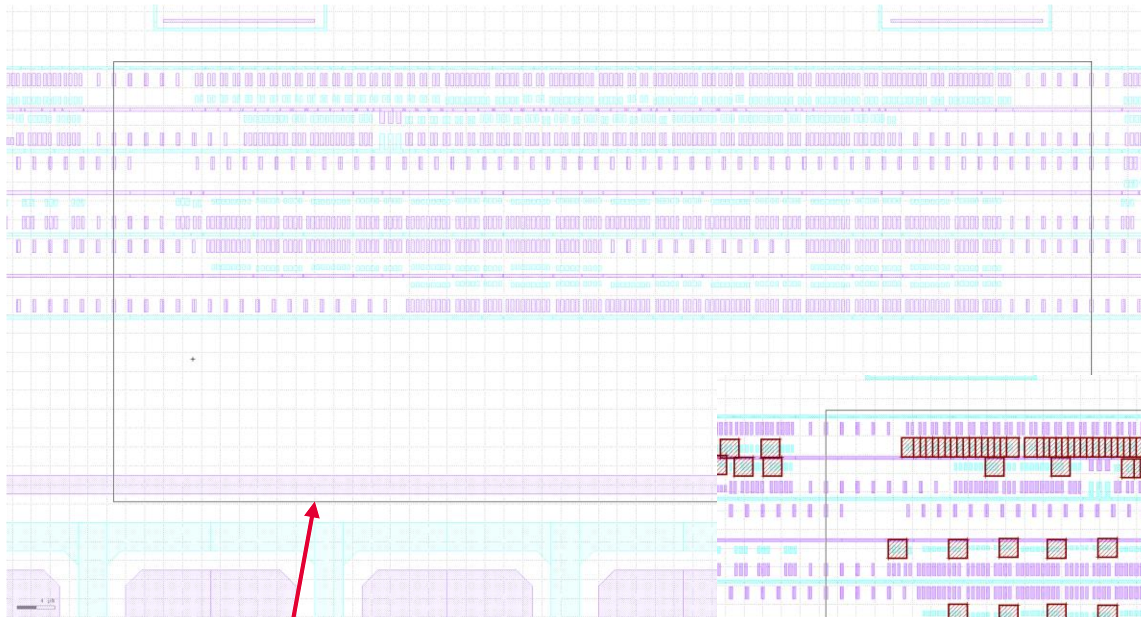
- It was proposed that metal traces in the package were impacting CDM charge distribution
  - Layout geometry from package was incorporated into the database used for CDM simulations
- Resulting simulations found physical failure locations matching cell where physical failures were located by FA



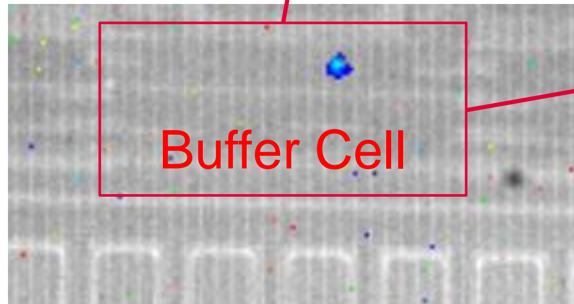
Physical Fail Location

Case 1 – Failure Not Found without Package

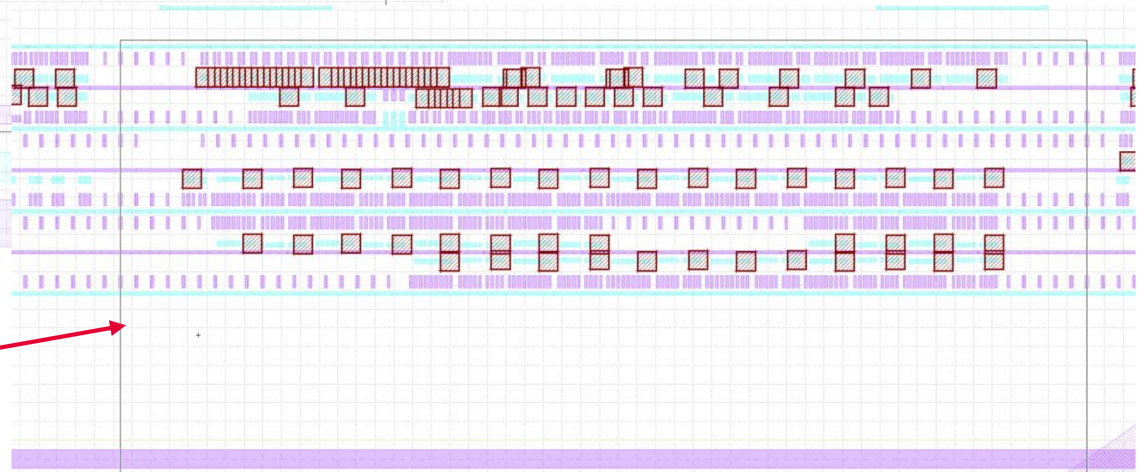
- Specific cell where failure occurred



No violations in cell when packaging not used in simulation



Photon Emission Analysis

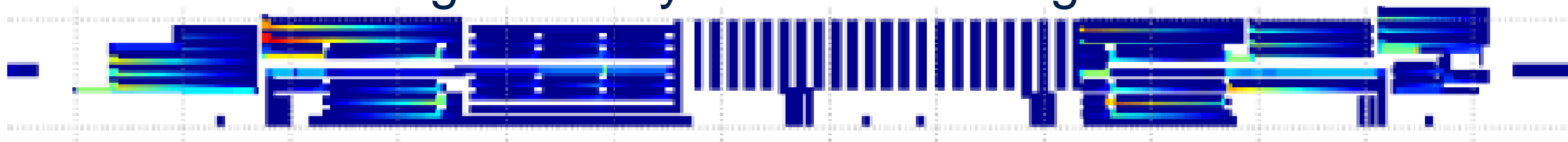


Numerous violations found when simulated with package data

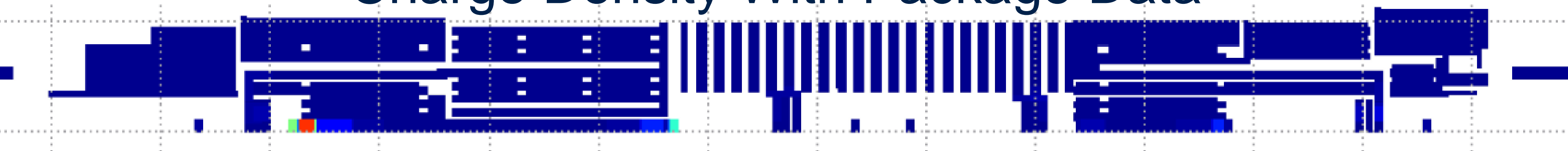
Case 1 – Failure Not Found without Package

- Charge distribution was impacted by presence of package layout metal
  - Top metal layer shown for IC
- Results from package included simulation showing concentrated charge storage density on specific nodes induced by FLR layout. Changes to the FLR layout corrected the violations.

Charge Density Without Package Data



Charge Density With Package Data



Case 2 – Failures Found Without Package

- Simulation of device was done with no package data
  - All pads from same die-net were shorted
- Results accurately identified failure location
- Other false errors were also present and some at higher stress value than actual failure point

Circuit Representation

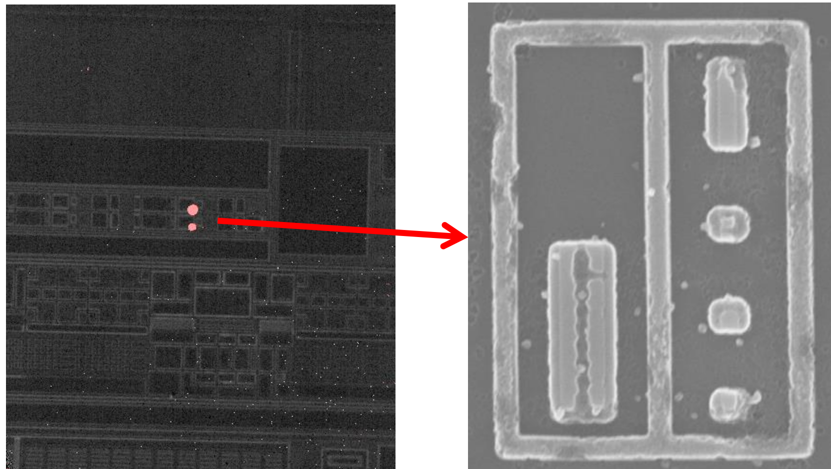
CDM Simulation

Physical Failure

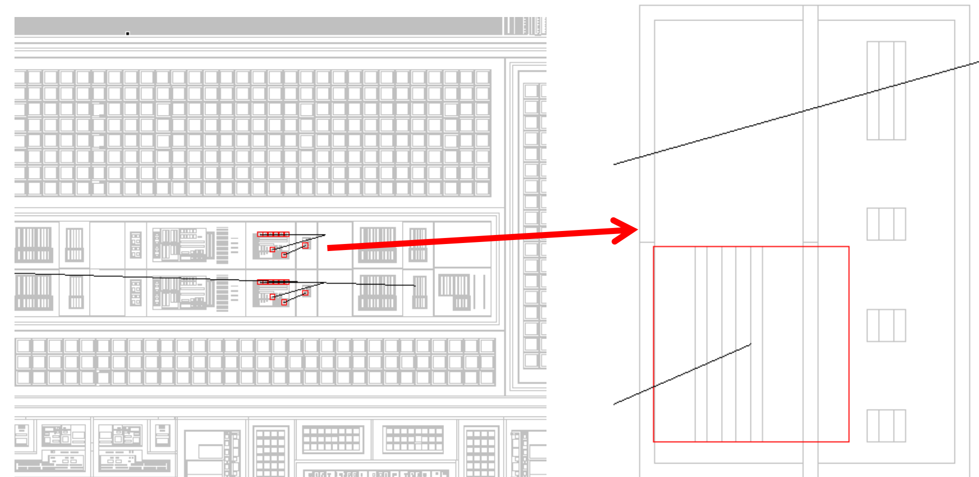
Case 2 – Failures Found Without Package

- Failure locations observed in silicon were also found by Esra simulation
- Inclusion of package data did not significantly reduce false violations nor change real violation detection

Photon Emission Analysis



Simulation Results



Conclusions

- Full chip CDM simulations can be a great tool for sign-off and failure analysis assistance.
- In considering the accuracy of CDM simulations there are cases where the package of a device can impact the results
- In cases where the package metal is much larger than top metal of the IC impacts to charge distribution can occur
  - It has been shown that through incorporation of package geometry into the IC database used for CDM simulations. Otherwise missed physical failures can be captured.
  - It was also shown that inclusion of package data does not degrade the simulation results when real violation locations can be found without it.

Conclusions

- While not all thin film packaging cases require this level of accuracy, it is important to be aware of all the possible caveats in performing full chip CDM simulations
  - Package netlist use insufficiencies
  - Impacts of package metal frame layout
    - Non-trivial conversion and inclusion in CDM simulation engines
  - CDM charge storage distribution impacts:
    - From IC metal geometry
    - From package metal geometry

Acknowledgements and References

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1. Dolphin Abessolo-Bidzo et al., "A Study of HBM and CDM Layout Simulations Tools", EOS/ESD 2018
2. Melanie Etherton et al., "Study of CDM Specific Effects for a Smart Power Input Protection Structure", EOS/ESD 2004
3. Dolphin Abessolo-Bidzo et al., "CDM Simulation Based on Tester, Package and Full Integrated Circuit Modeling: Case Study", IEEE Trans. on Electron Devices, vol. 59, pp. 2869 - 2875, Nov. 2012