

VCS with MVSIM

Comprehensive Low Power Simulation

Overview

Low power design techniques have rapidly evolved to manage power in semiconductor chips targeting a wide range of market segments from consumer to portable appliances, and even servers. Advanced low power techniques such as Power Gating, Retention, Low-Vdd Standby, and Dynamic Voltage Scaling (DVS) employ voltage control to manage power. Designs are partitioned into power domains that can be separately controlled by one or more of the low power design techniques. Increasingly stringent power requirements have necessitated the use of multiple supply voltages. Low power designs typically operate in different modes with each mode corresponding to one or more power states. Comprehensive verification of low power designs requires verification in all the power states as well as the specified transitions and order of transitions of the power states as the design moves from one operating mode to another. A single bug may cause functional failures in silicon.

Simulation Challenges for Low Power Designs

It is no longer sufficient to simulate a design assuming voltage to be a constant. Voltage changes during operation (such as in a design under low-Vdd standby, DVS or when using multiple supply voltages) and requires understanding of voltage values in simulation to correctly perform voltage resolution during simulation. Power state transitions require understanding of the dynamic nature of voltage and its effect on logic. All outputs are now a function of not only the inputs but also the voltage values. Traditional simulations will produce inaccurate results potentially allowing bugs to escape and manifest in silicon.

Multi-voltage designs have design components with multiple supply rails. Traditional simulators don't have the intelligence to understand the relationship between different supply voltages and what they drive, causing potential silicon failures that go undetected in simulation.

Power-on resets for low power designs involve turning power domains on in a sequential fashion where a previously powered up domain may help power up another domain. Understanding the voltage transitions and dependencies during power-on reset is essential to completely verifying a low power design.

VCS with MVSIM

VCS® with MVSIM performs voltage-level aware simulation with an understanding of voltage values and allows engineers to comprehensively verify correct behavior of designs that use voltage control techniques for power management.

Key Features and Benefits

- ▶ Accurate simulation of designs with Power Gating and many flavors of Retention lowers product cost
- ▶ Voltage-level aware simulation accurately verifies designs with Low-Vdd Standby and DVS
- ▶ Infrastructure to model and correctly simulate multi-rail designs leads to increased bug detection for multi-voltage designs
- ▶ Built-in, automated assertions derived from analysis of the design and power intent mitigate the risk of undetected bugs and increase verification productivity
- ▶ Automated coverage tracking and reporting helps track verification progress
- ▶ Production proven for IEEE 1801 [Unified Power Format (UPF)] shows support for industry-standard power intent format

VCS with MVSIM Flow

MVSIM is a co-simulator that works with functional simulators such as VCS™ through a Verilog Procedural Interface (VPI) Programming Language Interface (PLI). It takes in the same RTL or gate-level netlist representation of the design as VCS in either Verilog or VHDL and accepts the same test bench as VCS (now augmented for low power checks). Additionally, it allows the power intent to be specified in UPF. MVSIM understands all voltage events and accurately co-simulates the design to verify all power management functions. MVSIM outputs a log file and an error and warnings report for all violations related to multi-voltage checks.

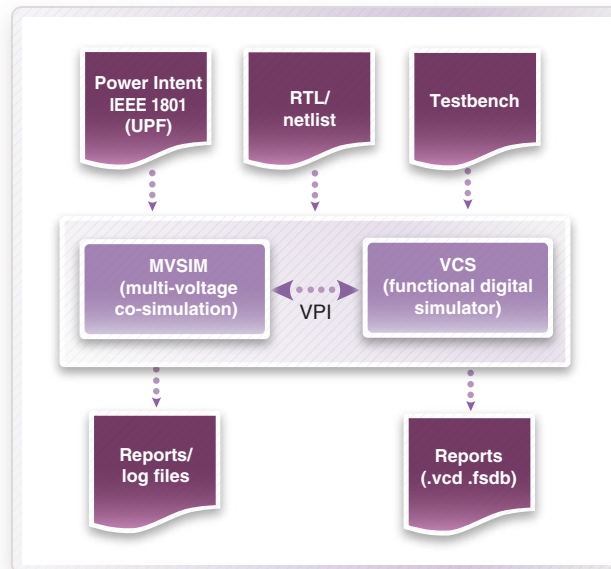


Figure 1: Low power simulation flow

Unique Value of VCS with MVSIM

- ▶ Voltage-level aware simulation detects bugs when multiple voltages transition simultaneously in a design or as a result of incorrect operation during a voltage ramping up or down. Voltage-level awareness helps verify the complex power-on-reset protocols typical of low power designs
- ▶ Comprehensive verification of voltage-control techniques, such as Low-Vdd Standby and DVS, that involve voltage value resolutions that can only be done by voltage-value simulation.
- ▶ Ability to associate different power domains with different supply voltages allows for accuracy of simulation of multi-voltage designs
- ▶ Built-in automated assertions based on years of low power verification expertise designed into the tools for all supported low power design techniques. The rich set of assertions is generated based on the design and power intent and help pin-point bugs. This feature replaces manual assertion generation, which is not scalable and is error-prone and tedious

Conclusion

Low power design techniques are increasingly used to combat leakage and dynamic power consumption. Multi-voltage designs require comprehensive verification coverage of all voltage-control techniques. VCS with MVSIM delivers voltage-level aware simulation that understands the voltage values and covers all power states, transitions and sequences. The product is production proven and widely adopted.

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