

# VCS

## Functional Verification Choice of Leading SoC Design Teams

### Overview

*Industry-leading designers of today's most advanced designs rely on the Synopsys VCS<sup>®</sup> functional verification solution for their verification environments. In fact, 90% of designs at 32nm and below are verified with VCS. Used by a majority of the world's top 20 semiconductor companies as their primary verification solution, VCS provides the high performance simulation engines, constraint solver engines, Native Testbench (NTB) support, broad SystemVerilog support, verification planning, coverage analysis and closure, and an integrated debug environment.*

*VCS has continually pioneered numerous industry-first innovations, and is now poised to meet the challenges and complexity of today's SoCs. With features such as such as constrained random testbench, SoC optimized compile flow, coverage, and assertions, VCS has the flexibility and capabilities that are critical for today's SoC design and verification teams' success.*

VCS offers industry-leading performance and capacity, complemented by a complete collection of advanced testbench, bug-finding, coverage and assertion technologies. VCS' multicore technology delivers a 2x verification speed-up and cuts down verification time by running the design, testbench, assertions, coverage and debug in parallel on machines with multiple cores. With its built-in debug and visualization environment; support for all popular design and verification languages, including Verilog, VHDL, SystemVerilog, OpenVera<sup>™</sup>, and SystemC<sup>™</sup>; and the VMM, OVM, and UVM<sup>™</sup> methodologies, VCS helps users develop high-quality designs. VCS' advanced bug-finding technologies include complete assertions and comprehensive code and functional coverage to find more design bugs faster and easier. VCS' powerful debug and visualization environment minimizes the turnaround time to find and fix design bugs. VCS, with MVSIM and MVRC, delivers innovative voltage-aware verification techniques to find bugs in modern low-power designs.

### High-performance, Full-featured, Native Testbench and Industry-Leading SystemVerilog Support

VCS' Native Testbench (NTB) technology provides built-in natively-compiled support for full-featured SystemVerilog and OpenVera testbenches, including object-oriented, constrained-random stimulus and functional coverage capabilities. VCS' industry-leading, high-performance constraint solver technology is powered by multiple solver engines that simultaneously analyze all user specified constraints to rapidly generate high-quality random stimulus that verifies corner case behavior. The constraint solver engines will find a solution to user constraints, if one exists, minimizing constraint conflicts and maximizing verification productivity.

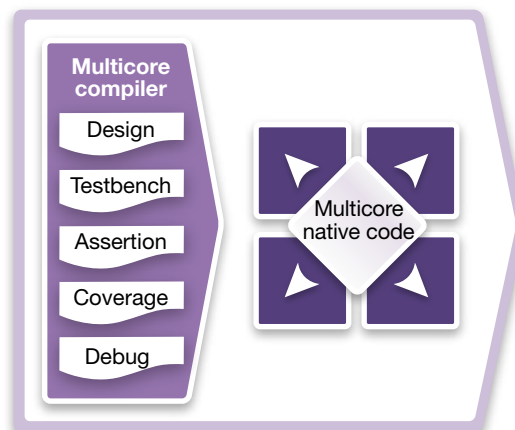


Figure 1: Multicore support

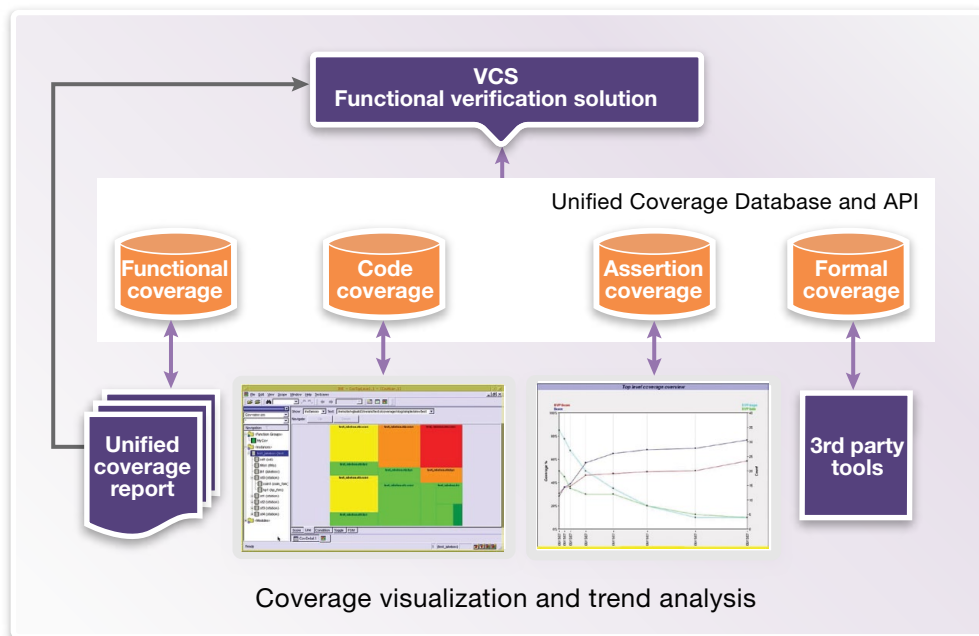


Figure 2: Unified coverage

VCS further expands its capabilities with Echo constraint expression convergence technology. Echo automatically generates stimuli to efficiently cover the testbench constraint space, significantly reducing the manual effort needed to verify large numbers of functional scenarios. Echo is a perfect fit for all teams using SystemVerilog testbenches with random constraints.

### Multicore Support

VCS' multicore technology allows users to cut verification time for long-running tests. It offers two robust use models: design-level parallelism (DLP) and application-level parallelism (ALP). DLP enables users to concurrently simulate multiple instances of a core, several partitions of a large design, or a combination of the two. ALP allows users to run testbenches, assertions, coverage, and debugging concurrently on multiple cores. The combination of DLP and ALP optimizes VCS' performance over multicore CPUs. VCS' multicore technology also supports design-level auto-partitioning,

Fast Signal Database (FSDB) parallel dumping, and switching activity interchange format (SAIF) parallel dumping.

### Comprehensive Coverage

VCS provides high-performance, built-in coverage technology to measure verification completeness. With its tight integration to Microsoft Word and Excel, Verification Planner offers a complete system to define and capture verification plans, and then monitor and manage coverage metrics throughout the verification and regression process. This helps verification teams quickly converge towards coverage goals. Comprehensive coverage includes code coverage, functional coverage, and assertion coverage. Unified coverage aggregates all aspects of coverage in a common database, thereby allowing powerful queries and useful unified report generation. The unified coverage database offers 2x to 5x improvement in merge times and up to 2x reduction in disk space usage, which is critical for large regression environments.

### Complete Assertion Technologies

The native assertion technology in VCS enables an efficient methodology for deploying design-for-verification (DFV) techniques. The built-in support of SystemVerilog and OpenVera assertions allows designers to easily adopt DFV and find more bugs quickly. A rich assertion-checker library and a unique library of Assertion IP make it even easier to deploy assertions across teams and improve verification quality. The assertions serve both simulation and formal property verification environments.

### Advanced Debugging and Visualization Environment

VCS includes the Discovery Visualization Environment (DVE), an advanced, full-featured debug and visualization environment. The DVE has been specifically architected to work with all of the advanced bug-finding technology in VCS and shares a common look and feel with other Synopsys graphical-based analysis tools. DVE enables easy access to design and verification data along with an intuitive drag-and-drop or menu-and-icon driven environment.

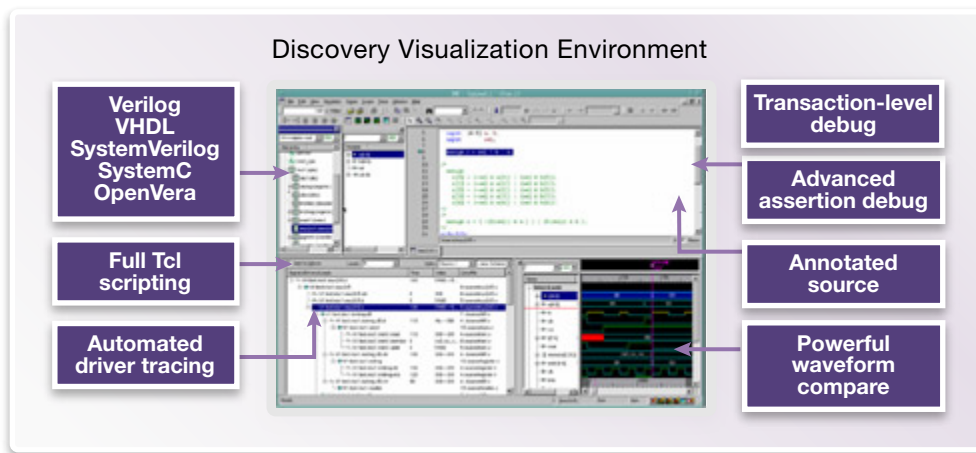


Figure 3: Discovery Visualization Environment (DVE)

Transaction-level debug is seamlessly integrated into DVE, allowing users to analyze and debug transactions in both list view and waveform view. Its debug capabilities include: tracing drivers, waveform compare, schematic views, path schematics, and support for the highly efficient Synopsys compact VCD+ binary dump format. It also provides elegant mixed-HDL (SystemVerilog, VHDL and Verilog) and SystemC/C++ language debugging windows, along with next-generation assertion tracing capabilities, that help automate the manual tracing of relevant signals and sequences.

DVE further provides powerful capabilities for SystemVerilog testbench debug (including VMM and UVM methodologies) with several key features, including detailed constraint debug and constraint conflict resolution. DVE is tightly integrated with Verification Planner and VCS' unified coverage database, enabling verification teams to view and manage coverage information, create reports, and troubleshoot and resolve coverage bottlenecks throughout the verification and regression process.

TCL support is provided for interaction or batch control and skin/menu customization. Unified command language support provides a common set of commands for all tools, languages and environments, making it easy to deploy new technology across design teams.

### Support for VMM, OVM, and Accellera UVM

VCS' powerful testbench engines are complemented by support for VMM, OVM 2.1.1, and the Accellera UVM methodologies. With these methodologies, users adopt industry best practices to get the optimum results from VCS. In addition, the VMM methodology provides a number of applications, such as Register Abstraction Layer (RAL) and others, to cut down on the time it takes to set up a powerful verification environment.

VCS' support for Accellera UVM also includes access to the VMM/UVM interoperability kit, which enables the use of VMM with UVM and vice versa. In addition, the VMM methodology provides a number of applications, such as Register Abstraction Layer (RAL) and others, to cut down on the time taken to set up a powerful verification environment. All the VMM applications, a detailed reference manual and examples are provided with the VCS solution.

### Synopsys Verification IP

Synopsys provides a broad spectrum of Verification IP to verify SoC protocols and interfaces. Synopsys VIP's have been proven in production by hundreds of verification teams on thousands of projects to verify IP blocks, IP integration, SoC interconnect and complete SoCs. The Synopsys Verification IP's supports advanced SystemVerilog-based testbenches including methodology support for VMM, OVM, and UVM. It includes features to simplify testbench development, provide higher coverage and improve simulation runtime. VCS is further optimized for the performance, capacity, debug, and coverage features of Synopsys Verification IP's.

**For more information about VCS, please visit:**

<http://www.synopsys.com/VCS>

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