

Galaxy Constraint Analyzer

Look-ahead constraint analysis for the Galaxy Implementation Platform

Overview

Galaxy™ Constraint Analyzer improves designer productivity through look-ahead timing constraint analysis and debug technology tuned for the Synopsys Galaxy Implementation Platform. Early feedback on constraint quality leads to more efficient runtimes and better quality of results in Synopsys' Design Compiler® synthesis and IC Compiler physical implementation tools.

Galaxy Constraint Analyzer provides an intuitive interactive environment for designers to quickly assess the correctness and consistency of timing constraints, helping eliminate trial-and-error iterations during implementation and thereby resulting in more predictable schedules and reduced design cost.

Whether it is run pre- or post-layout, Galaxy Constraint Analyzer uses PrimeTime® constraint interpretation and propagation technology to improve constraint quality input to the implementation and signoff process.

Galaxy Constraint Analyzer Solution

The rapid increase in design size and complexity, as well as the widespread reuse of IP design blocks, has led to a major increase in the size and complexity of timing constraint specification files. Ensuring high-quality timing constraints is paramount to efficient design implementation, especially during handoffs between teams. Incomplete, inconsistent or conflicting constraints can cause optimization and implementation tools to run ineffectively or to never converge. To address this challenge, Galaxy Constraint Analyzer provides a comprehensive set of rule checks designed to maximize the efficiency of Design Compiler synthesis and IC Compiler physical implementation.

Look-ahead Constraint Analysis Technology

Galaxy Constraint Analyzer uses technology based on Synopsys' golden PrimeTime timing engine to ensure correct interpretation and propagation of constraints. This gives designers a signoff-correlated view of the constraints ahead of each step of the design implementation process. By delivering comprehensive constraint analysis on 10-million-gate designs in a matter of minutes, combined with a unique set of interactive analysis and debug capabilities, Galaxy Constraint Analyzer helps designers quickly identify and fix constraint issues in hours versus days.

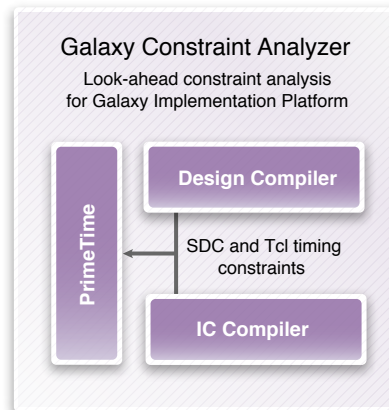


Figure 1: Galaxy Constraint Analyzer

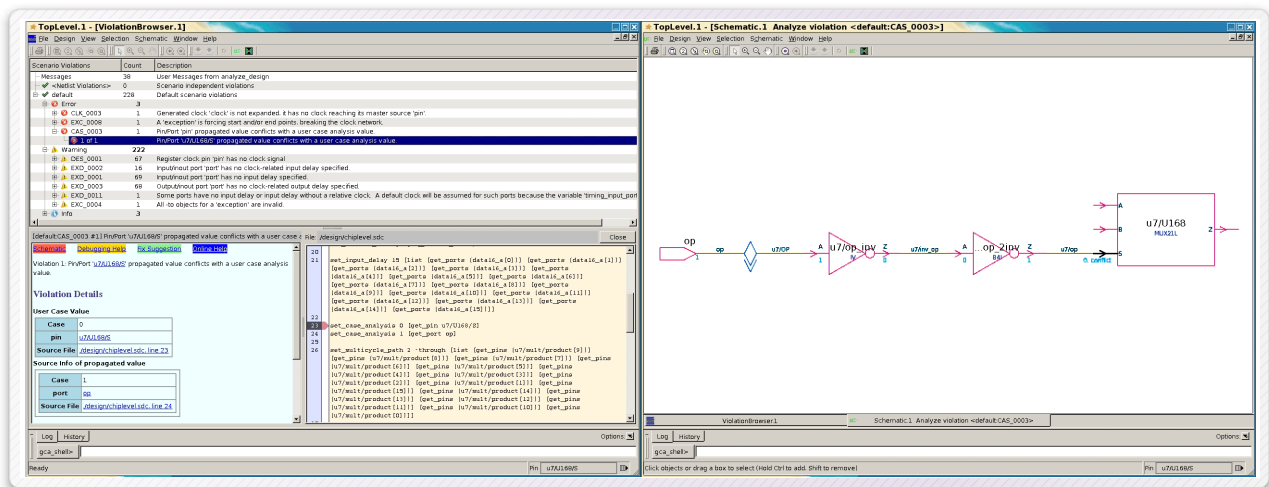


Figure 2: Galaxy Constraint Analyzer Debug Environment

Key Features

Powerful rule checking

Galaxy Constraint Analyzer includes comprehensive timing rule checks which cover pre- and post-layout timing conditions. Users have the ability to create rule classes which allow them to customize the rulesets for a given phase in the design process.

- ▶ Supports version 1.8 SDC
- ▶ Supports Tcl from PrimeTime, Design Compiler and IC Compiler
- ▶ Extensible with user-defined rules written in Tcl
- ▶ Supports Galaxy-specific rule checks to help users create constraints which maximize efficiency in Design Compiler, IC Compiler and PrimeTime

Best-in-class debug solution

Unique to Galaxy Constraint Analyzer is its extensive support for debugging of constraint violations. The tool is designed to allow users to debug reported violations in real time using the interactive graphical user interface.

All violations are displayed in the violation browser, including custom rules generated by the end user.

- ▶ Includes cross-probing to Tcl, SDC and schematic
- ▶ Comprehensive reporting including debugging guidance and constraint fixing recommendations
- ▶ Fast runtimes enabling interactive analysis and debug sessions

When the source of a violation is identified, the user can simply rerun that rule check to verify that the proposed constraint fix will work as expected and fix the violation.

Easy to deploy

Galaxy Constraint Analyzer shares a common core user interface with the Galaxy Implementation Platform tool suite. Scripts from Design Compiler, IC Compiler and PrimeTime can be run without modifications.

Since constraint interpretation is shared with PrimeTime, new users have no difficulties providing conclusive feedback to Design Compiler and IC Compiler users on violating constraints.

- ▶ Common look-and-feel with other Galaxy implementation and signoff tools
- ▶ No modifications required to run Design Compiler, IC Compiler and PrimeTime scripts

- ▶ Intuitive interface with user-selectable levels of reporting
- ▶ Plugs in easily to existing Galaxy implementation and signoff flows

Specifications

File format support

Galaxy Constraint Analyzer supports the following industry-standard formats

- ▶ Netlist: Verilog
- ▶ Constraint: SDC 1.8, Design Compiler, IC Compiler and PrimeTime Tcl timing constraints
- ▶ Libraries: Liberty™ format

Platform support

Supported Platforms:

- ▶ AMD64
- ▶ Linux32 4.0
- ▶ Suse 32
- ▶ Suse 64

For more information about this product, sales, support services or training, please contact your local Synopsys representative or call 1-800-388-9125



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