

The conceptual flow is mapped into an actual process flow as it is this which is certified as DO-254 compliant. It is worth noting that it is the flow itself which is subject to certification, not the individual tools used to engineer the flow.

Synopsys provides a range of applications that can be used to create such compliant processes. A typical flow may resemble that of Figure 2.

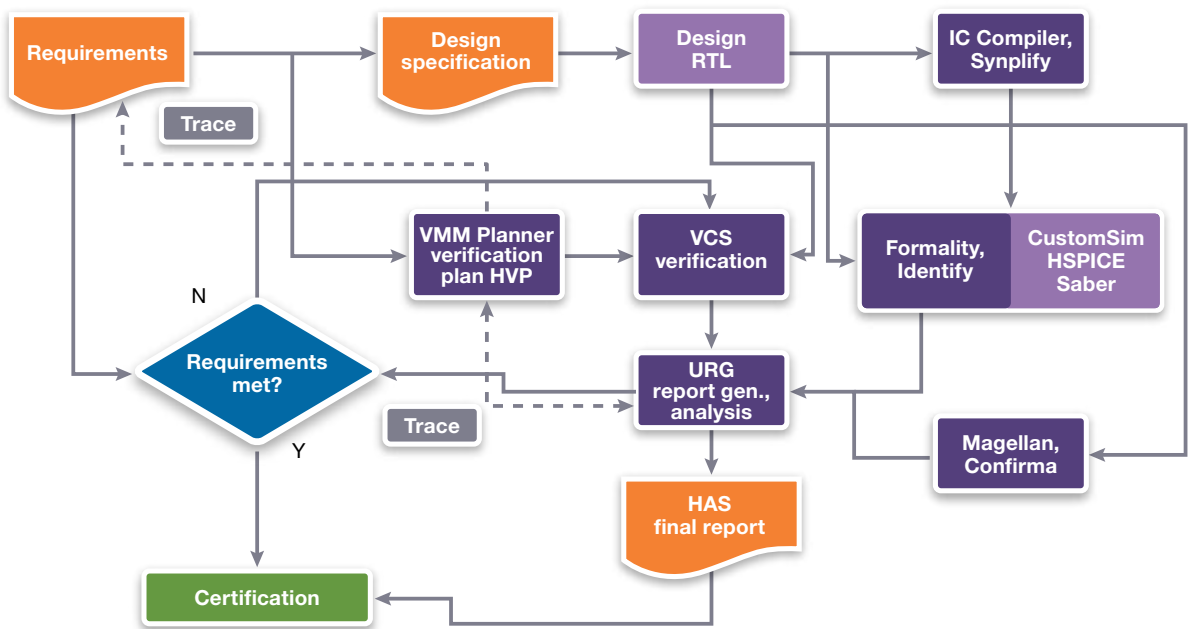


Figure 2: DO-254 design flow with Synopsys tools

An earlier whitepaper, “Understanding DO-254 Compliance for Airborne Hardware Design and Verification Flows” discusses achieving a DO-254 compliant flow in more general terms. However, a key principle remains constant for successful DO-254 compliant flows: **verification results** (e.g. simulation waveforms, regression status, coverage figures) **must be traceable and linked to the formal requirements**. The process of traceability may be either automated or manual. This whitepaper focuses on using Synopsys applications to maximize the automation of this aspect of DO-254 compliance.

The Verification Process in a DO-254 Compliant Flow

The verification process demonstrates that the formal requirements which are used to specify the design have been validated. There are several aspects to successfully implementing a DO-254 compliant verification process. The DO-254 standard itself does not specify or dictate the choice of tools or methodologies use in the process; it, instead, requires that the final design implements the formal requirements. These key aspects are

- ▶ Creation / capture of formal requirements
- ▶ Producing a verification plan the specifies how the requirements are verified
- ▶ Demonstrating all requirements have been validated

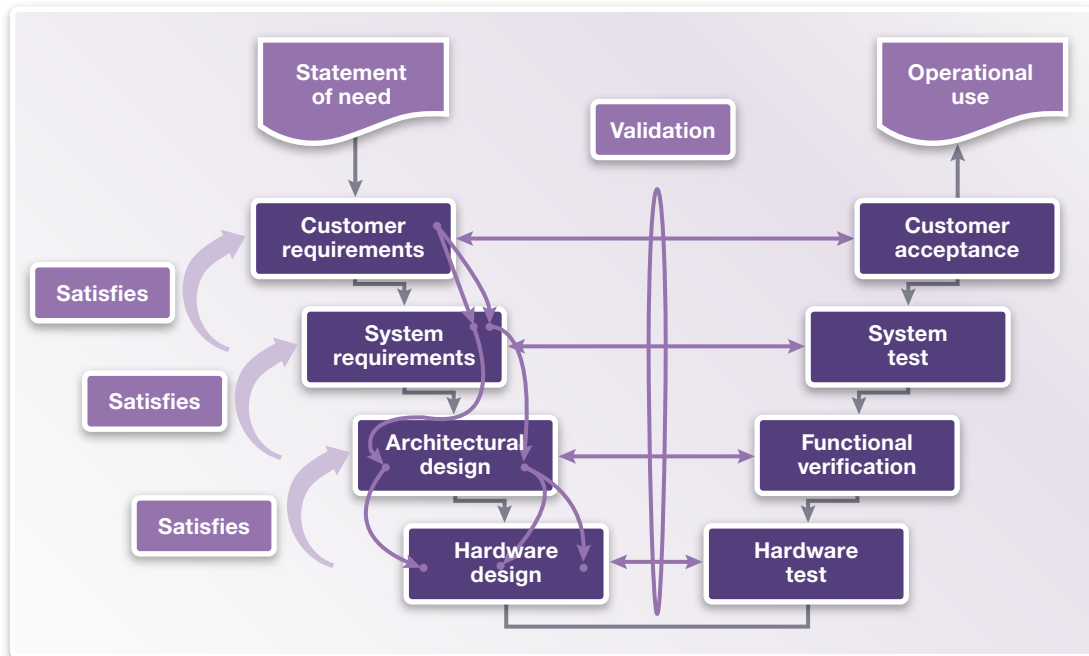


Figure 3: Requirements Validation Process

The formal requirements capture process was described in the earlier whitepaper *“Understanding DO-254 Compliance for Airborne Hardware Design and Verification Flows”*. Typically IBM’s DOORS program is used to capture the design requirements, though other tools of varying sophistication have been used. If DOORS is used to capture the requirements it is natural to use this program to also capture the verification plan. With the advent of constrained-random coverage-driven verification, this format is not ideally suited for the process of tracking the progress of validation the requirements through simulation. It is more efficient to be able to convert the verification plan into a form which can be integrated with the progress tracking items in the verification environment such as code, functional and assertion coverage.

It is important to establish verification metrics in order to be able to demonstrate that verification has been completed. A variety of metrics, correlating to a variety of verification methods, might be necessary. Capturing these metrics from all tests and all simulation runs into a single database allows results to be gathered into one report. This provides a single automated report that describes all aspects of test results. A key factor in achieving this is ensuring that requirement validation can be captured as Functional Coverage points and Temporal Assertions. These effectively become linked to the requirements themselves in order to provide the traceability demanded in a DO-254 compliant verification process.

Creating a Hierarchical Verification Plan

Requirements capture, planning and traceability

All verification process flows need a verification plan in order to track the progress of the validation of the design. Traditionally, this plan is created in a somewhat ad-hoc way which makes it difficult to both track progress and ensure that verification results are related back to the functional design features. VMM Planner provides a special language, HVP, that allows creation of a hierarchical verification plan. This is a very full-featured system and goes beyond what is necessary to provide a DO-254 compliant verification flow. This section will focus on the most typical use-case in such flows where other tools need to be integrated into the overall methodology.

DO-254 stipulates that a design must be specified using formal requirements. The first step in any DO-254 development is to capture these requirements, often using a special-purpose tool such as DOORS. Requirements are written hierarchically, meaning that a high level requirement may be composed of several simpler ones. Demonstrating that all the lower level requirements have been satisfied proves that the parent requirement has been met as well.

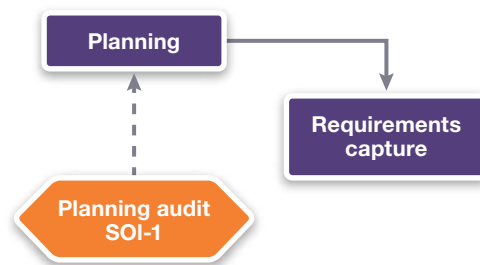


Figure 4: SOI-1 Audit -to Capture Steps

To provide for traceability between the requirements to be verified and their actual validation, a special-purpose tool such as DOORS is often employed to capture the test plan and, sometimes, the test procedures (though it is not uncommon for both to be specified in the same document). The test plan describes what is to be tested and the test procedures describe what the actual tests are, together with their associated correctness criteria.

The test procedures are most often mapped to assertions and covergroup definitions when using a constrained-random methodology for verification. Since the original requirements are specified hierarchically (i.e. by functional unit) the testplan naturally follows this structure.

A testplan created in DOORS is not directly usable in a verification environment as there is no mechanism to annotate the results into the DOORS database. However, traceability can be maintained if there is still linkage from the original requirements to the test plan (and test procedures). This means that any data exported from DOORS still retains its traceability.

Synopsys VMM Planner has the facility to create a verification plan directly using Hierarchical Verification Plan (HVP), a comprehensive model that allows you to describe a verification plan in a hierarchical structure. The verification plan contains vital information to document the overall verification process, such as feature declarations, attributes, goals, and appropriate metrics. Attributes are named values specified in the plan, whereas metrics are those named values automatically annotated from the results of VCS simulation. Metrics can be such features coverage information extracted from merged simulation runs, and can also include other project specific information. Even though some of this data isn't necessarily of direct interest to a DO-254 compliant flow, values as version control numbers can be useful to include for archival purposes.

Since the verification plan and test procedures in a DO-254 compliant project must be linked to the original requirements, the most common methodology is to export these plans from DOORS or equivalent tools into a form which can be annotated with the appropriate values for the metrics.

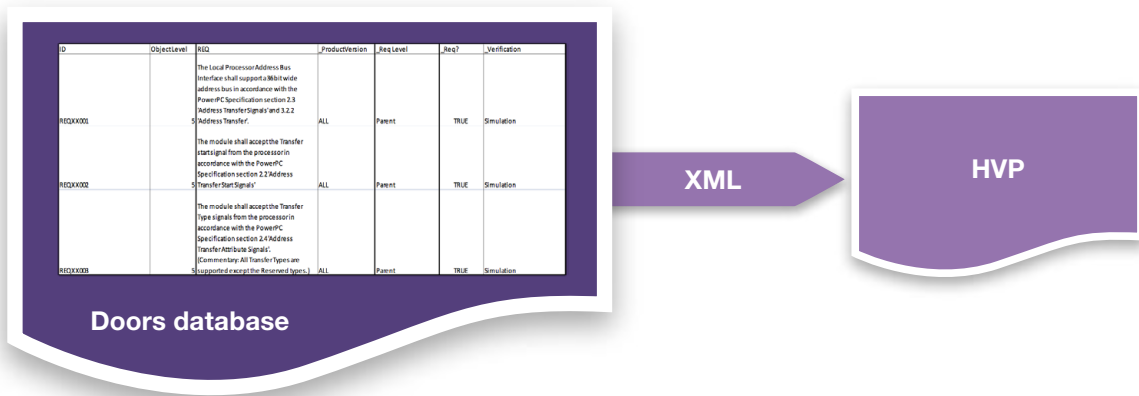


Figure 5: DOORS export via XML to HVP

VMM Planner recognizes the initial spreadsheet as the implicit verification plan. This is produced by exporting the verification plan described in DOORS in a portable format (e.g. an XML spreadsheet).

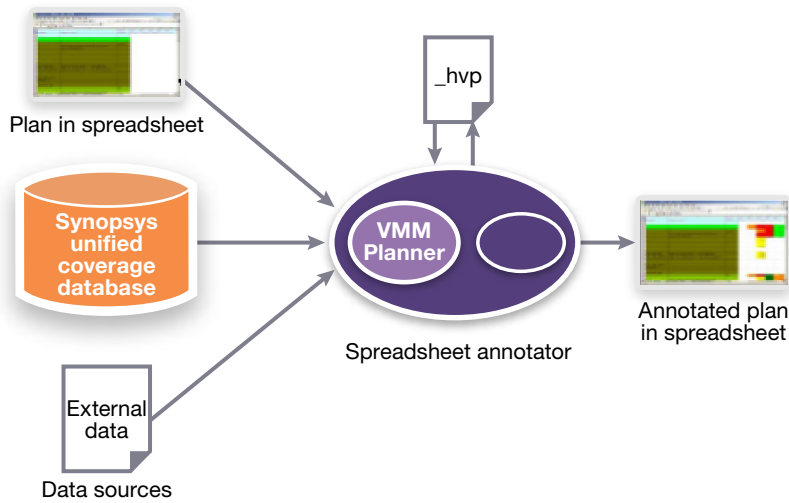


Figure 6: VMM Planner spreadsheet annotation flow

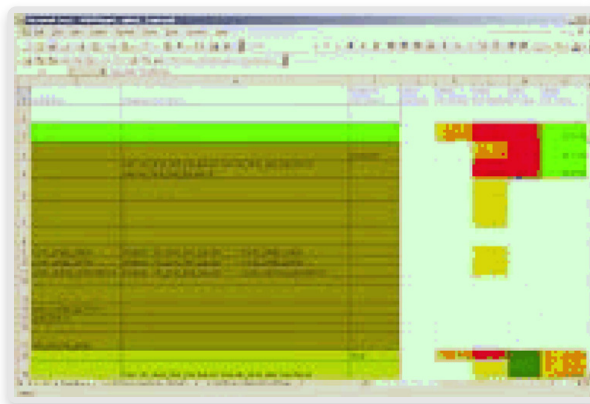


Figure 6: Exported implicit verification plan with annotation

Special meta-tags are used to describe the annotation points, and should be included as objects in the DOORS database to maintain their linkage with the original requirements. Such inclusion also promotes common maintenance, under the same version control regime, as the rest of the formal documents. Generated documents, such as the exported XML spreadsheet are always re-created when the original source documents change, reducing the need for revision control. However, it is still viewed as a best practice to apply revision control to all artifacts, regardless of whether they can be automatically recreated.

Integrating DO-254 Compliant Verification Requirements using VMM Planner and VCS

VCS is used to provide the results that can be annotated into the metrics documented in an exported verification plan. Data is available from the Synopsys Unified Coverage Database so that results can be aggregated across simulation runs with different random seeds.

ID	Object Level	REQ	ProductVersion	_Req Level	_Req?	_Verification
REQXX001	5	The Local Processor Address Bus interface shall support a 36 bit wide address bus in accordance with the PowerPC Specification section 2.3 'Address Transfer Signals' and 3.2.2 'Address Transfer'.	ALL	Parent	TRUE	Simulation
REQXX002	5	The module shall accept the Transfer start signal from the processor in accordance with the PowerPC Specification section 2.2 'Address Transfer Start Signals'.	ALL	Parent	TRUE	Simulation
REQXX003	5	The module shall accept the Transfer Type signals from the processor in accordance with the PowerPC Specification section 2.4 'Address Transfer Attribute Signals'. [Commentary: All Transfer Types are supported except the Reserved types.]	ALL	Parent	TRUE	Simulation

Figure 8: Requirements exported from DOORS into Excel

Figure 9 shows the contents of the Excel file converted into an HVP, the format required by Synopsys' VMM Planner. Coverage and/or assertion metrics have been associated with each requirement.

hvp plan PowerPC interface	feature	subfeature	\$description	value ppc_if .Group	value ppc_if .Assert	value ppc_if .Assert	measure ppc_if .source
plan							
	PowerPC Interface						
		RCQXX001 Address Bus	The Local Processor Address Bus interface shall support a 36 bit wide address bus in accordance with the PowerPC Specification section 2.3 'Address Transfer Signals' and 3.2.2 'Address Transfer'.				group instance ppc_ if.address_ tenure
		RCQXX002 Transfer Start	The module shall accept the Transfer start (TSF) signal from the processor in accordance with the PowerPC Specification section 2.2 'Address Transfer Start Signals'.				property ppc_ if.assert_ transfer_ start
		RCQXX003 Transfer Type	The module shall accept the Transfer Type signals from the processor in accordance with the PowerPC Specification section 2.4 'Address Transfer Attribute Signals'. [Commentary: All Transfer Types are supported except the Reserved types.]				group instance ppc_ if.transfer_ type

Figure 9: Requirements in an HVP spreadsheet

It is assumed in these examples that a sophisticated, self-checking verification environment using constrained random, coverage-driven verification techniques (such as those provided by the VMM) has been created. This combination of a VMM Planner based methodology and a VMM environment coupled with VMM-compliant verification IP (see Fig. 9) provides a proven means of building a DO-254 compliant verification environment faster and with greater confidence versus other methods.

A traditional directed-test verification environment may still be used, if assertions are already present in the RTL code. In this case, the unified coverage database is used to store assertion results; code coverage metrics, which will be necessary for proving compliance to DO-254 Level A and B design criticality, are also kept. The results of verification from formal tools such as Magellan™ are also available in the database, and can be annotated back to the metrics in the exported verification plan.

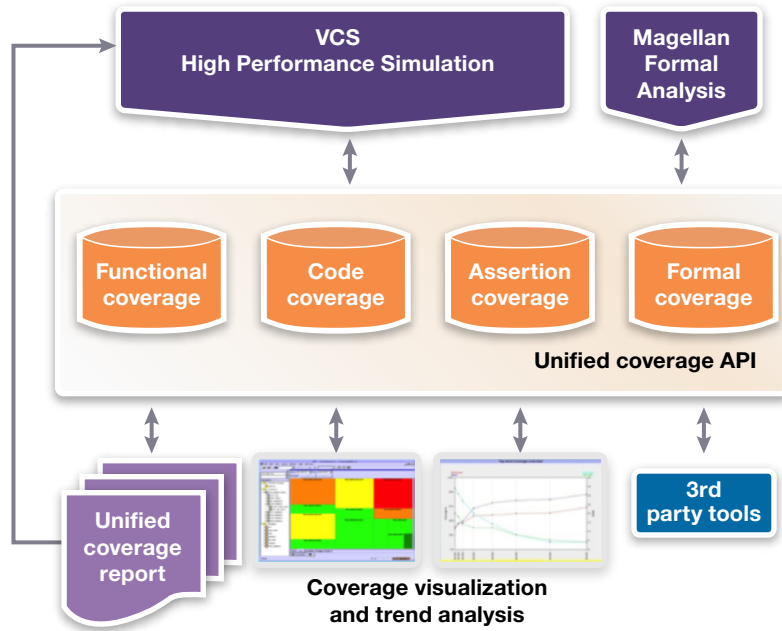


Figure 10: Synopsys unified coverage database

Once the environment is complete, the process of regression testing begins, with the goal of achieving the verification objectives specified as metrics in the HVP.

Requirements Coverage and Traceability

Traceability is critical for DO-254 compliance, and documentation detailing the depth and breadth of the verification effort is needed to obtain DO-254 certification.

VMM Planner becomes a great ally, then, to achieving DO-254 compliance. It allows VCS to merge and annotate simulation results onto the metrics in the HVP. Using this combination, verification progress can be easily tracked and documented and the associated environment, including its tests and constraints, may be modified as necessary to achieve verification closure.

Reports are needed to show coverage progress, and the tests and random seeds that were used to attain it. These reports are always required by verification managers but once the coverage goals have been achieved and verification is deemed to be complete, the reports and annotated verification plan are the evidence that a DER will require to certify successful DO-254 compliance.

As mentioned above, reports generated via VCS/URG/VMM Planner are needed for DO-254 certification, as they prove to a DER that verification of the design has been complete. They form the final link in the traceability chain from the original design formal requirements, through the associated verification plan, the exported implicit verification plan, all the way to an annotated verification plan in HVP format. Because these final stages are automated and repeatable (via running the same set of regression tests with a consistent export and annotation process), the essential traceability that is so key to DO-254 compliance is maintained.

Any reporting mechanism that completes this traceability chain may be used but the full power of the Synopsys unified coverage database can be used if the URG (Unified Report Generator) tool is used for this part of the process.

Results Data Management and Analysis using URG

The figures below illustrate the flow (Figure 11) and some of the data analysis and visualization features (Figure 12) of the URG. These features are particularly useful in helping achieve verification closure as they can be used to determine which aspects of verification have not been completed yet and may suggest where to apply directed test cases for those areas where constrained-random testing did not achieve the desired coverage.

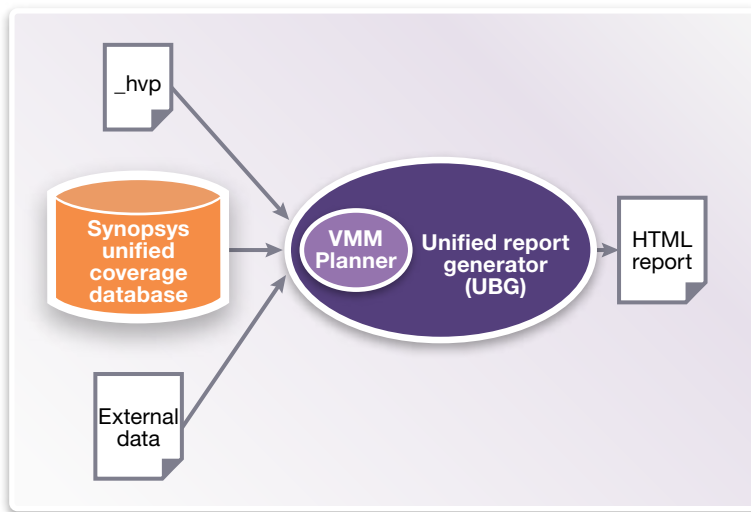


Figure 11: Unified report generator flow

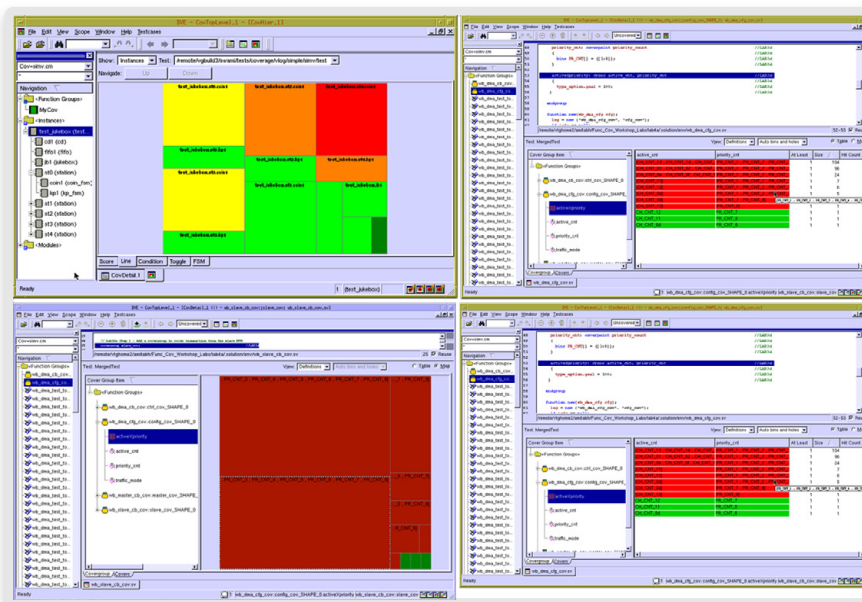


Figure 12: Results visualization

Using URG also allows analysis of coverage statistics, and can indicate which tests contributed to this coverage. This allows an optimal regression suite to be built which will achieve the highest level of verification coverage for the minimum amount of simulation resources, for example.

Tests

[dashboard](#) | [hierarchy](#) | [modlist](#) | [groups](#) | [tests](#) | [asserts](#)

Total Coverage Summary

SCORE	LINE	COND	FSM	ASSERT	GROUP
94.15	98.88	93.62	90.00	88.24	100.00

Total tests in report: 3

Data from the following tests was used to generate this report

simv/test
simv/results

Figure 13: Coverage report generated by URG

URG also can be used to build web pages of the results, providing an alternate vehicle to display, manage, and present the results of the verification process.

Conclusion

The development of a Hierarchical Verification plan can facilitate an easier, more efficient path to implementing, documenting, and obtaining certification of your DO-254 flow. Using the combination of Synopsys' VCS and Magellan verification engines with the VMM Planner and Uniform Report Generator provides the verification engineer a powerful combination: a widely adopted, market leading simulation engine with (powerful) tools for defining and tracking progress of a complex verification plan and documenting its completeness.

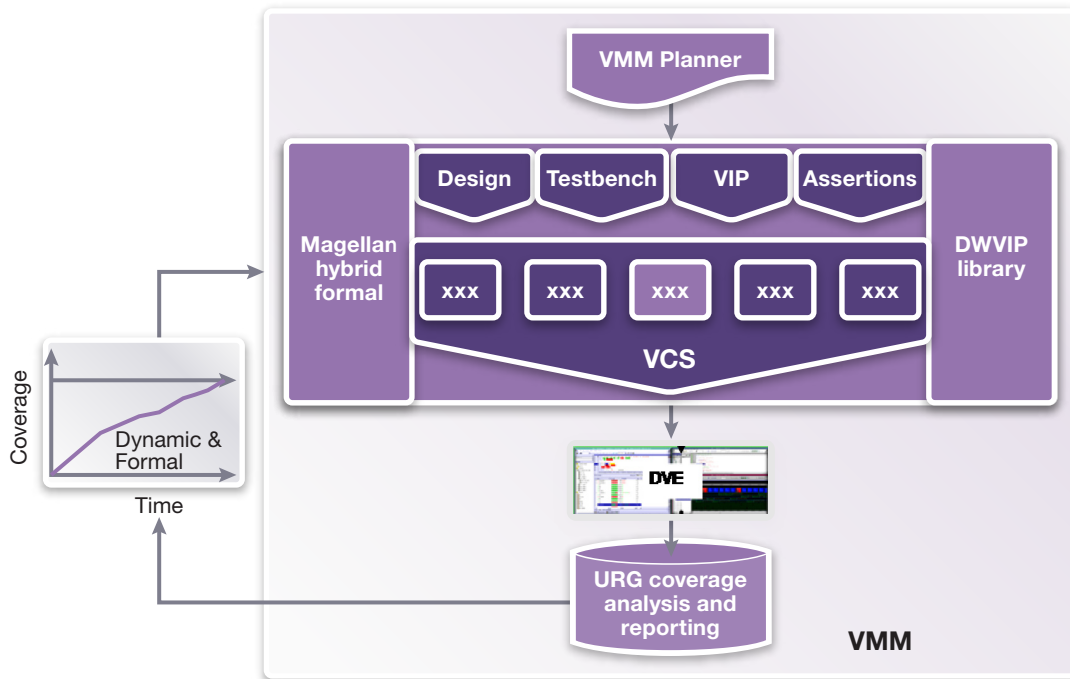


Figure 14: Verification flow with VCS

Resources

For further information, visit the DO-254 User's Group at www.do-254.org. A copy of the specification itself can be purchased from the RTCA organization at <http://www.rtca.org/onlinecart/product.cfm?id=194>.

Newcomers to the DO-254 process may benefit from training and through the engagement of consultants. Skilled in advanced verification techniques and familiar with the DO-254 process, consultants can provide the head start needed to achieve maximum productivity and project success.